US Nation Stage of PCT/JP00/05595 --26. The polishing pad for a semiconductor wafer according to Claim 21, wherein the surface layer is foamed of foamed polyurethane.--

--27. A method for polishing a semiconductor wafer, wherein the polishing is performed by using the polishing pad according to Claim 21.--

--28. A method for polishing a semiconductor wafer, wherein the polishing is performed by using the polishing pad according to Claim 22.--

--29. A method for polishing a semiconductor wafer, wherein the polishing is performed by using the polishing pad according to Claim 23.--

--30. A method for polishing a semiconductor wafer, wherein the polishing is performed by using the polishing pad according to Claim 20.--

--31. A method for polishing a semiconductor wafer, wherein the finish polishing is performed while a concentration of zinc compounds is kept to 200ppm or less in the position where the semiconductor wafer is in contact with the polishing pad.--

REMARKS

Claims 21-31 are pending. Claims 21-31 are added. Prompt and favorable consideration on the merits is respectfully requested.

Respectfully submitted,

William P. Berridge Registration No. 30,024

Thomas J. Pardini Registration No. 30,411

WPB:TJP/zmc Date: April 26, 2001

n

OLIFF & BERRIDGE, PLC P.O. Box 19928 Alexandria, Virginia 22320 Telephone: (703) 836-6400 DEPOSIT ACCOUNT USE
AUTHORIZATION
Please grant any extension
necessary for entry;
Charge any fee due to our
Deposit Account No. 15-0461